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Article (Published Version)

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Citation: Appl. Phys. Lett. **110**, 113504 (2017); doi: 10.1063/1.4978531
View online: http://dx.doi.org/10.1063/1.4978531
View Table of Contents: http://aip.scitation.org/toc/apl/110/11
Published by the American Institute of Physics

Solution-processed p-type copper(I) thiocyanate (CuSCN) for low-voltage flexible thin-film transistors and integrated inverter circuits

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(Received 24 November 2016; accepted 1 March 2017; published online 17 March 2017)

We report on low operating voltage thin-film transistors (TFTs) and integrated inverters based on copper(I) thiocyanate (CuSCN) layers processed from solution at low temperature on free-standing plastic foils. As-fabricated coplanar bottom-gate and staggered top-gate TFTs exhibit hole-transporting characteristics with average mobility values of 0.0016 $cm^2\ V^{-1}\ s^{-1}$ and 0.013 $cm^2\ V^{-1}\ s^{-1}$, respectively, current on/off ratio in the range 10^2–10^4, and maximum operating voltages between −3.5 and −10 V, depending on the gate dielectric employed. The promising TFT characteristics enable fabrication of unipolar NOT gates on flexible free-standing plastic substrates with voltage gain of 3.4 at voltages as low as −3.5 V. Importantly, discrete CuSCN transistors and integrated logic inverters remain fully functional even when mechanically bent to a tensile radius of 4 mm, demonstrating the potential of the technology for flexible electronics. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4978531]

Flexible thin-film transistors (TFTs) hold great potential for numerous emerging applications, including flexible and paper-like displays,[1] wearable and textile integrated systems,[2,3] smart labels and intelligent packaging,[2,4] epidermal devices,[5] electronic skins,[6] as well as imperceptible, biomimetic, and transient implants.[7–9] In recent years tremendous advances have been achieved through the use of metal oxide semiconductors as the channel materials[10] as they combine processing versatility[11] and high electron carrier mobility[12] leading to realization of numerous functional systems including large-area digital[13–15] and analog[15–17] circuits composed of hundreds of TFTs.[13] Despite the impressive progress, however, further developments are hampered by the lack of p-type semiconductors with performance and stability comparable to those found in their n-type counterparts.[18] So far only a handful of research groups have reported flexible p-type TFTs based on either SnO_x[18–22] or CuO_x[23–25] metal oxide semiconductors. Even though a hole mobility value up to 5.87 $cm^2\ V^{-1}\ s^{-1}$ has been reported,[20] the vacuum-deposition techniques (e.g., DC[19,20,24] or RF[21–23] sputtering) often used rely on relatively high annealing temperatures >150 °C, which in turn render the technologies incompatible with inexpensive plastic substrates. As a result, to date there is a continuous quest for alternative p-type materials that can be grown at low temperatures from solution-phase.[10] One such semiconductor is the copper(I) thiocyanate (CuSCN)—an inorganic molecular compound—that exhibits intrinsic p-type conductivity, excellent transparency in the visible range due to its large optical band gap, and low-temperature solution-processability.[11,26,27] Recently, Pattanasattayavong *et al.* have reported the fabrication of TFTs and unipolar inverters based on solution-processed layers of CuSCN at temperatures as low as 80 °C. Resulting TFTs and circuits showed excellent p-channel operation with hole mobility values in the range of 0.01–0.1 $cm^2\ V^{-1}\ s^{-1}$ and signal gains of up to 2.[26,27] In spite of the low processing temperature, the presented devices have been fabricated on rigid or substrates.

Here, we report the development of flexible low-voltage CuSCN TFTs and logic integrated inverters processed from solution at extremely low temperatures of ≤80 °C. Discrete bottom-gate bottom-contact and top-gate bottom-contact CuSCN transistors fabricated on freestanding plastic foils exhibit unipolar p-channel behaviour with hole mobility values of 0.0016 $cm^2\ V^{-1}\ s^{-1}$ and 0.013 $cm^2\ V^{-1}\ s^{-1}$, respectively. The characteristically reliable device operation allows realization of integrated unipolar voltage inverters (NOT gates) with both active and passive loads yielding input signal gains of up to 3.4 at a supply voltage down to −3.5 V. Importantly, both discrete devices and integrated inverters remain fully operational even under tensile bending radii

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down to 4 mm, clearly demonstrating the potential of CuSCN as a p-channel semiconductor for the emerging field of flexible transparent electronics.

Coplanar bottom-gate bottom-contact (BG-BC) transistors were fabricated on a free-standing flexible polyimide (PI) foil (surface area of $7.6 \times 7.6\,cm^2$). The 50 μm-thick Kapton PI was chosen because of its low thermal (12×10^{-6} K^{-1}) and humidity (9×10^{-6}%RH^{-1}) expansion coefficients, its high glass transition temperature ($T_g \sim 360\,°C$), as well as its relatively low surface roughness (rms $\sim$ 4 nm).[28] Figure 1(a) shows the schematic device cross-section of the flexible BG-BC CuSCN TFTs. To provide a sufficient adhesion of the device layers to the flexible foil, 50 nm-thick layers of SiN_X were grown on both sides of the PI substrate using plasma-enhanced chemical vapor deposition (PECVD). Next, a 30 nm layer of Cr was e-beam evaporated and patterned into bottom-gate contacts using standard UV photolithography and wet etching. Following, a 25 nm-thick Al_2O_3 gate dielectric (dielectric constant $\varepsilon_R = 9.5$) was grown by atomic layer deposition (ALD) at 150 °C. Gate contact holes through the dielectric were structured by photolithographic wet etching.[25] Subsequently, source and drain (S/D) contacts consisting of 10 nm/50 nm of Ti/Au were e-beam evaporated using lift-off. Prior to the semiconductor growth, the substrate was diced into chips of $1.5 \times 1.5\,cm^2$. The diced chips were sequentially cleaned by ultra-sonication in acetone and isopropanol baths for 5 min and subjected to UV/ozone treatment for 30 min. The active layer solution was prepared by dissolving the CuSCN precursor (Aldrich) in dipropyl sulfide (Merck, 99%) at a concentration of 20 mg ml^{-1}. Undissolved material was removed by centrifuging and filtering the CuSCN solution at room temperature.[26] The solution was then spin-coated and annealed at 80 °C for 15 min under nitrogen atmosphere, yielding a 15 nm-thick CuSCN layer. The resulting BG-BC TFTs had a channel length (L) and width (W) of 20 μm and 1400 μm, respectively.

In order to investigate the charge transport characteristics of as-deposited CuSCN layers as well as their compatibility with solution-processed gate dielectrics for flexible transistor applications, we incorporated CuSCN films into the TG-BC TFT architecture [Figure 1(b)] and spin-coated the polymer dielectric. The CuSCN active layer was grown using the same process described above, whereas Au S/D and Al gate contacts were formed by thermal evaporation in high vacuum (10^{-6} mbar) through shadow masks. As gate dielectric, poly(vinylidene fluoride-trifluoroethylene-chlorofluoroethylene) [P(VDF-TrFE-CFE)] layers were utilized. P(VDF-TrFE-CFE) is a high-k relaxor ferroelectric polymeric dielectric (ε_R up to $\approx$60), which can be solution-processed at low temperatures.[26,29] The P(VDF-TrFE-CFE) with composition of 56/36.5/7.5 mol% was dissolved in methyl-ethyl-ketone (MEK) at a concentration of 30 mg ml^{-1}.[26] P(VDF-TrFE-CFE) films were spin-coated and subsequently annealed at 60 °C for 3 h in nitrogen, resulting in a $\sim$160 nm-thick layer. The channel dimensions of the resulting TG-BC TFTs were L = 40 μm and W = 1500 μm.

The surface morphology of the as-spun CuSCN films was studied by atomic force microscopy (AFM) in tapping mode. Figures 1(c) and 1(d) display the topographic images of CuSCN layers coated on PI/SiN_x/Cr/Al_2O_3 (for the BG-BC structure) and PI/SiN_x (for the TG-BC structure), respectively, while Figure 1(e) shows the height distributions of the two layers. The CuSCN layer on Al_2O_3 exhibits the common feature of elliptic domains, which have been previously reported for CuSCN films on glass, and also has a similar surface roughness (r.m.s value of $\sim$1.7 nm).[26,30] The CuSCN domains for the layer deposited on SiN_x appear longer and thinner, almost whisker-like, and the roughness increases slightly to 3.5 nm. The effects of the underlying layers and deposition conditions on the morphology of CuSCN films are still unclear and will be subject to further investigation. However, previous and current results show that the field-effect mobilities in CuSCN-based transistors fabricated on different substrates or from different solvents[26,27,31,32] are comparable to the values reported here. Although those CuSCN layers exhibited slightly different morphologies in terms of grain shape and size, their dimensions were in the same order of magnitude (10–100 nm). The nanocrystallinity and the associated high density of grain boundaries most

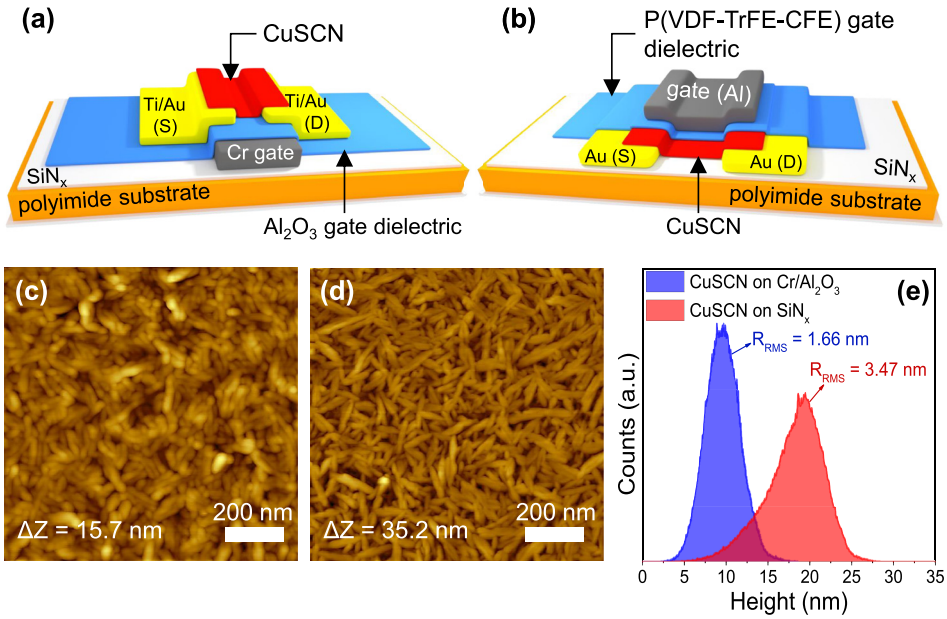

FIG. 1. Schematic cross-section of the (a) coplanar bottom-gate bottom-contact (BG-BC) and (b) staggered top-gate bottom-contact (TG-BC) copper(I) thiocyanate (CuSCN) TFTs fabricated on free-standing polyimide substrates. AFM topography images of CuSCN films spin-coated onto (c) a polyimide/SiN_X/Cr/Al_2O_3 and (d) a polyimide/SiN_X surface with the corresponding height distributions shown in (e).

likely play an important role at limiting the hole transport. Further work would be required to elucidate the exact nature of the charge transport and its dependence on the layer morphology/microstructure.

The charge transport properties of the as-deposited CuSCN films were investigated using the flexible BG-BC and TG-BC TFT architectures in dry nitrogen. Figure 2 displays a representative set of the transfer (a) and the output (b) characteristics measured for a representative flexible BG-BC CuSCN TFT. The device exhibits low voltage operation (≥ -3.5 V) and excellent hole transporting (p-channel) characteristics. Analysis of the transfer characteristics yields a current on/off ratio (I_{ON}/I_{OFF}) of $>10^2$, a threshold voltage (V_{TH}) of -1.5 V, a sub-threshold swing (SS) of $\sim$1.7 V/dec, and a saturation field-effect hole mobility (μ_{SAT}) of 0.0016 cm^2 V^{-1} s^{-1}. The gate leakage (I_G) remained always <10 nA and as such did not interfere with the device operation. Analysis of the electrical characterization of 6 different TFTs across several different substrates yielded μ_{SAT} and V_{TH} of 1.5 ($\pm$0.4) $\times 10^{-3}$ cm^2 V^{-1} $s^{-1}$and -1.5 ($\pm$0.1) V, respectively, showcasing the good uniformity of the fabrication process employed. Upon exposure to ambient air at room temperature (RH $\sim$ 55%) for 30 min, the CuSCN TFTs remained fully functional and showed a 45% reduction in the effective mobility and a threshold voltage shift of approximately -400 mV. Importantly, the initial transistor characteristic is fully recovered when the devices are re-exposed to nitrogen air, suggesting that no chemical changes are taking place within the CuSCN layer and that the observed effect is most likely due to physisorption of atmospheric oxidants, e.g., water and oxygen.

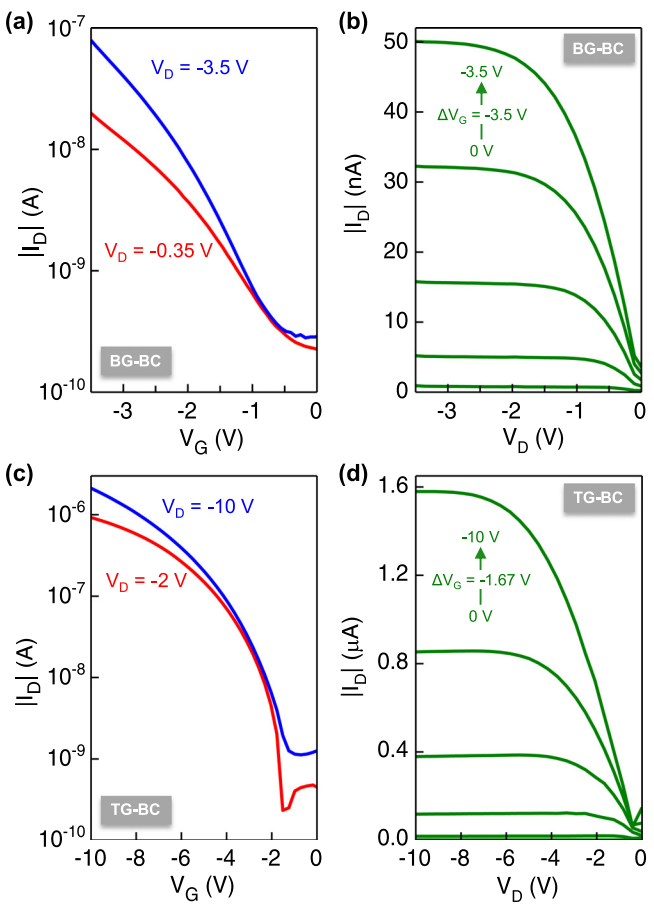

FIG. 2. Transfer (a) and output (b) characteristics of a flexible low-voltage BG-BC CuSCN p-type TFT with Al_2O_3 gate dielectric (W = 1400 μm and L = 20 μm). Transfer (c) and output (d) characteristics of a flexible low-voltage TG-BC CuSCN p-type TFT with P(VDF-TrFE-CFE) gate dielectric (W = 1500 μm and L = 40 μm).

Nevertheless, the mobility values obtained here are generally lower than the average μ_{SAT} of 0.01–0.1 cm^2 V^{-1} s^{-1} reported previously for TG-BC CuSCN TFTs fabricated on rigid substrates.[26] This is most likely attributed to the unfavorable coplanar BG-BC architecture,[33] combined with the potentially higher concentration of trap states at the Al_2O_3/CuSCN interface. When similar CuSCN films were incorporated in an optimized staggered TG-BC flexible TFT geometry employing a high-k P(VDF-TrFE-CFE) gate dielectric [Figure 2(c)], the hole saturation mobility and the on/off current ratio reach higher values up to 0.013 cm^2 V^{-1} s^{-1} and 2×10^3, respectively. As shown in Figures 2(c) and 2(d), flexible TG-BC CuSCN TFTs exhibit clear p-type characteristics, with low-voltage operation and clear channel current saturation.

In addition to the electrical performance, the mechanical bendability of any emerging TFT technology is expected to play a key role in its widespread application. In order to test the mechanical properties of the CuSCN TFTs, we attached the flexible substrates to a double-sided adhesive tape and wound them around a metallic cylinder rod of 4 mm radius [Figure 3(a)], so that tensile strain was applied parallel to the transistor channel. Figures 3(b) and 3(c) display representative sets of transfer characteristics measured for a flexible BG-TB (b) and a TG-BC (c) CuSCN TFTs while flat (solid lines) and bent (dashed lines) to a tensile radius (R) of 4 mm. Evidently, both types of CuSCN TFTs remain fully operational even when bent to 4 mm radius (which corresponds to a strain $\varepsilon \sim 0.58\%$ calculated using the approximation given by Gleskova *et al.*[34]) and show only minor and reversible changes in their performance characteristics. In particular, under tensile strain both BG-BC and TG-BC CuSCN TFTs exhibit a small reduction in μ_{SAT} (down to 0.0013 cm^2 V^{-1} s^{-1} and 0.01 cm^2 V^{-1} s^{-1}, respectively) and a slight positive shift ($\sim$70 mV) in V_{TH}. The use of a low gate-source voltage together with a 5-min interval between the TFT characterization while flat and while bent allows minimizing the influence of electric stress. The slightly reduced μ_{SAT} and the positively shifted V_{TH} could possibly be attributed to the formation of micro-cracks within the nanocrystalline CuSCN layer. Compared with previously reported bending experiments of TFTs based on polycrystalline In_2O_3[35] and nanocrystalline ZnO,[35,36] our CuSCN devices result in the same trend with 83% smaller variations at comparably low bending radii. Specifically, In_2O_3- and ZnO-based devices exhibit 98% to 99% reduction in μ_{SAT} and 1.2 V to 1V shift in V_{TH} while bent to 10 mm radii whereas our CuSCN TFTs only show 16% μ_{SAT} reduction and 70 mV V_{TH} shift at 4 mm. Also, re-flattening of the devices allows closing up the micro-cracks and therefore leads to a full recovery of the un-strained TFT performance. Nevertheless, bending to even smaller radii induces cracks that permanently harm the device operation. These results demonstrate the superior mechanical stability of our p-type crystalline CuSCN TFTs and their suitability for application in large-area flexible electronics.

The promising CuSCN TFT characteristics prompted us to explore this interesting technology for application in

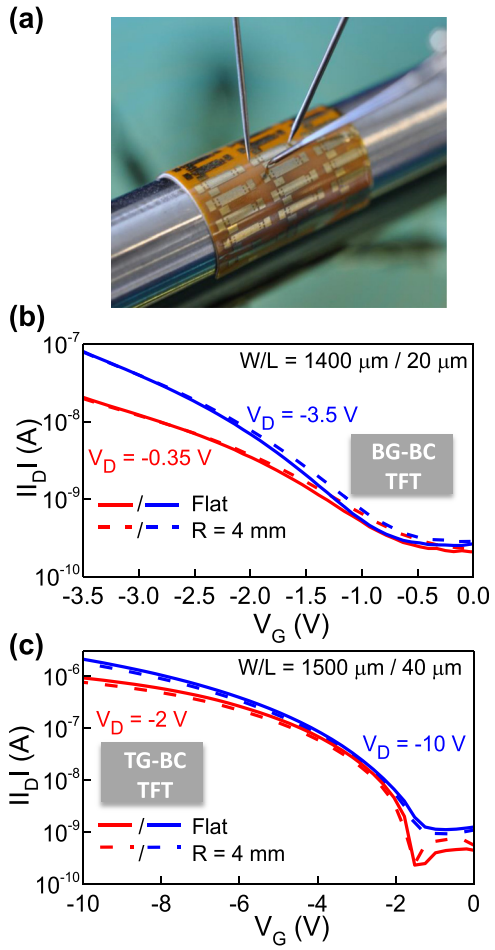

FIG. 3. (a) Photograph of a flexible CuSCN TFT mechanically bent to a tensile radius of 4 mm. Transfer characteristics of a BG-BC (b) and a TG-BC (c) CuSCN TFTs measured while flat (solid lines) and subsequently bent (dashed lines) to a tensile radius of 4 mm.

flexible integrated inverters. Figure 4(a) shows a photograph of an as-processed flexible substrate ($7.6 \times 7.6\,cm^2$ in size) containing various CuSCN-based NOT gates based on active [Figure 4(b)] and passive [Figure 4(c)] circuitry. Electrical characterization of discrete CuSCN transistors was used to design logic inverters with centered midpoint voltages $V_M \approx V_{SS}/2$. Integrated inverters with active load consisted of a driving and a load CuSCN TFTs with W/L of 3200 μm/20 μm and 450 μm/20 μm, respectively, whereas the inverter with passive load combines a driving TFT with W/L = 2100 μm/20 μm and a passive load resistor with resistance R = 170 kΩ. All the CuSCN TFTs were fabricated using the more practical BG-BC device architecture whereas the resistor used in the passive load inverter was implemented using the Cr gate metal itself (resistivity $\rho = 1.16 \times 10^{-6}$ Ω·m). All the interconnections were integrated into the Ti/Au S/D metallization layer, eliminating the need for additional processing steps.

Figure 4(d) shows the voltage transfer characteristic (VTC) and the corresponding signal gain (G) of the NOT gate in active configuration measured at a supply voltage V_{SS} of −3.5 V. The inverter exhibits G = 3.4, an almost centered V_M of −1.5 V, and a good output swing (output high voltage $V_{OH} = -0.2$ V and output low voltage $V_{OL} = -2.9$ V) even at a low V_{SS} of −3.5 V. Inverters with passive load [Figure 4(e)] based on flexible CuSCN TFTs and Cr resistor yield similar performance (G = 2.5 and $V_M = -1.95$ V), demonstrating the high degree of flexibility of our technology as well as the reproducibility of the CuSCN TFTs. Furthermore, both NOT gates were fully functional while mechanically bent to 4 mm tensile radius [Figures 4(d) and 4(e)]. The small variations observed in the CuSCN inverter performance parameters (changes in G and V_M of ±4% and ±100 mV, respectively) are attributed to the strain-induced changes in the TFT/resistor performance. Additionally, inverters with passive loads remained operational after being exposed for 30 min to ambient air, demonstrating good stability towards atmospheric oxidants.

In summary, we have developed flexible p-channel TFTs and unipolar integrated NOT gate circuits based on CuSCN p-type semiconductor layers processed from solution-phase at 80 °C. The resulting CuSCN transistors exhibit low operating

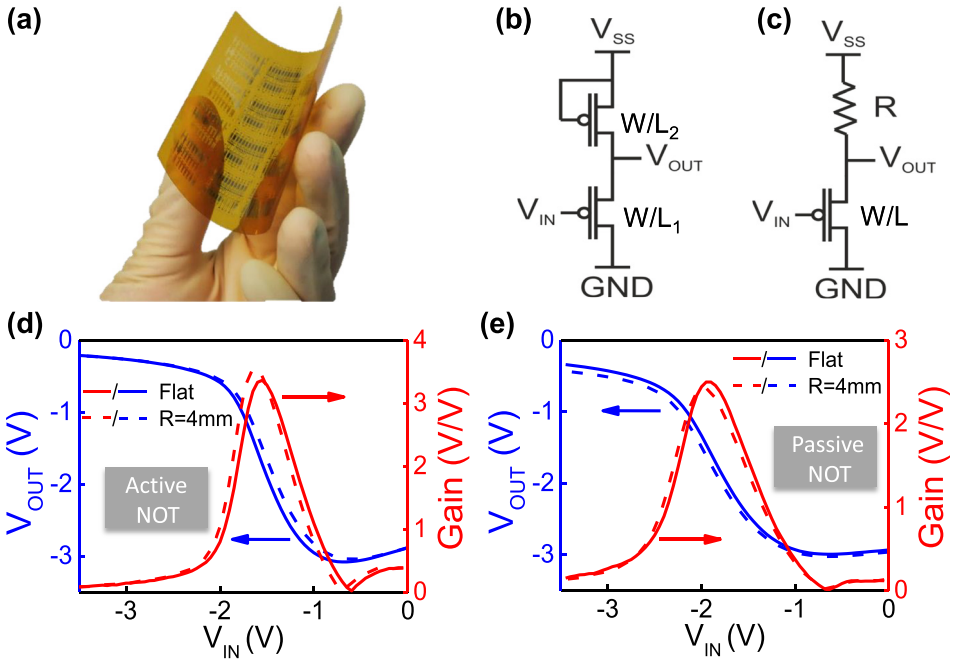

FIG. 4. (a) Photograph of a fully processed flexible substrate comprising several CuSCN-based integrated circuits. Circuit schematics of a unipolar voltage inverter (NOT gate) in active (b) and passive (c) load configuration based on p-channel TFTs. Voltage transfer characteristics and corresponding signal gain curves for NOT gates based on active (d) and passive (e) circuitry employing CuSCN p-type TFTs, measured at a supply voltage (V_{SS}) of −3.5 V while flat (solid lines) and bent (dashed lines) to a tensile radius of 4 mm. The inverter in active configuration comprises a driving and a load CuSCN TFT with W/L of, respectively, 3200 μm/20 μm and 450 μm/20 μm, whereas the NOT gate with passive load comprises a driving TFT with W/L = 2100 μm/20 μm and a passive load 170 kΩ resistor.

voltages with a maximum hole mobility of 0.013 $cm^2\ V^{-1}s^{-1}$ and on/off channel current ratio of $\sim 10^3$. Different unipolar NOT gates made using a combination of CuSCN TFTs and load resistors exhibit excellent inverting characteristics with input signal gain up to 3.4 and operating voltages down to −3.5 V. Finally, CuSCN TFTs and inverter circuits were shown to remain fully functional even when mechanically bent to a tensile radius of 4 mm. This work further asserts CuSCN as a promising p-type transparent semiconductor for application in flexible, large-area electronics.

The authors would like to acknowledge N. Wijeyasinghe from Imperial College London for her support during the device and circuit fabrication and characterization.

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